

What is claimed is:

1 1. An apparatus comprising:

2 a micro-operation generator to receive a predicated instruction that indicates a plurality of
3 destination registers;

4 the micro-operation generator further to generate a plurality of micro-operations that
5 implement the instruction;

6 the micro-operation generator further to decompose the instruction into the plurality of
7 micro-operations such that each of the micro-operations indicates a single destination
8 register.

1
1 2. The apparatus of claim 1, wherein

2 the plurality of micro-operations includes one or more standard micro-operations to
3 provide the basic functionality indicated by the instruction.

1
1 3. The apparatus of claim 1, wherein

2 the plurality of micro-operations includes one or more predication-support micro-
3 operations.

1
1 4. The apparatus of claim 3, wherein:

1 the one or more predication-support micro-operations includes a conditional move micro-
2 operation for each destination register indicated by the instruction, where the conditional
3 move micro-operation is to select between a first and second proposed output value based on
4 the value of a qualifying predicate associated with the instruction.

5
1 5. The apparatus of claim 4, wherein:

2 the first proposed output value is the incoming value of the associated destination
3 register; and

4 the second proposed output value is a computed value.
5

1 6. The apparatus of claim 4, wherein:

2 the first proposed output value is the incoming value of the associated destination
3 register; and

4 the second proposed output value is a constant value.
1

1 7. The apparatus of claim 6, wherein the instruction is a compare instruction.
1

1 8. The apparatus of claim 7, wherein the instruction is an “or” form compare
2 instruction.
3

1 9. The apparatus of claim 7, wherein the instruction is an “and” form compare
2 instruction.

1 10. The apparatus of claim 7, wherein the instruction is an “and”-complement form
2 compare instruction.

1 11. The apparatus of claim 7, wherein the instruction is an “or”-complement form
2 compare instruction.

1 12. The apparatus of claim 4, wherein:
2 the instruction is a parallel compare instruction.

1 13. The apparatus of claim 12, wherein:
2 the one or more predication-support micro-operations include a first conditional move
3 micro-operation for a first destination register indicated by the parallel compare instruction;

4 the one or more predication-support micro-operations also include a second conditional
5 move micro-operation for a second destination register indicated by the parallel compare
6 instruction;

7 the first proposed output value for the first conditional move micro-operation is the
8 incoming value of the associated destination register;

9 the second proposed output value for the first conditional move micro-operation is a first
10 constant;

11 the first proposed output value for the second conditional move micro-operation is the
12 incoming value of the associated destination register;

13 the second proposed output value for second first conditional move micro-operation is a
14 second constant.

1
1 14. The apparatus of claim 13, wherein the instruction is an “and.orcm” form of a
2 parallel compare instruction.

1
1 15. The apparatus of claim 12, wherein the instruction is an “or.andcm” form of a
2 parallel compare instruction.

1
1 16. The apparatus of claim 3, wherein:
2 the one or more predication support micro-operations includes an append operation to
3 append a qualifying predicate value to a proposed output value.

1
1 17. The apparatus of claim 3, wherein:
2 the instruction is a load instruction; and
3 the one or more predication support micro-operations includes an append operation to
4 append a qualifying predicate value to a load address.

1

1 18. The apparatus of claim 3, wherein:

2 the instruction is a store instruction; and

3 the one or more predication support micro-operations includes an append operation to
4 append a qualifying predicate value to a store address.

1

1 19. A system comprising:

2 a memory to store an instruction that indicates a plurality of destination registers; and

3 a processor coupled to the memory;

4 wherein the processor includes a microcode engine to generate, for the instruction, a
5 series of micro-operations, wherein each of the micro-operations indicates a single
6 destination operand and a maximum of two source operands.

1

1 20. The system of claim 19, wherein:

2 the memory is a DRAM.

1

1 21. The system of claim 19, wherein:

2 the instruction is predicated; and

3 the micro-code engine is further to generate, for each of the destination registers indicated
4 by the instruction, a micro-operation to conditionally move one of two proposed values into
5 the destination register.

1
1 22. The system of claim 21, wherein:

2 the micro-code engine is further to generate, for each of the destination registers indicated
3 by the instruction, a micro-operation to conditionally move one of two proposed values into
4 the destination register.

1
1 23. The system of claim 22, wherein:

2 a micro-operation to store an incoming value of the destination register is further to
3 append a qualifying predicate value for the instruction with the stored incoming value.

1
1 24. A method comprising:

2 receiving an instruction that indicates a plurality of destination registers; and
3 generating a plurality of standard micro-operations for the instruction, wherein each
4 of the standard micro-operations indicates a single destination register.

1
1 25. The method of claim 24, further comprising:

2 generating, if the instruction is predicated, a plurality of predication-support micro-
3 operations for the instruction.

1
1 26. The method of claim 25, wherein generating a plurality of predication-support
2 micro-operations further comprises:

3 generating a conditional move micro-operation for each destination register indicated by
4 the instruction.

1
1 27. The method of claim 26, wherein generating a conditional move operation further
2 comprises:

3 if the instruction indicates a known constant as a first potential output value, generating a
4 micro-operation that receives a second potential output value as an input, wherein execution
5 of the micro-operation is to cause a processor to move either the constant value or a second
6 potential output value into a destination register.

1
1 28. The method of claim 26, wherein generating a conditional move operation further
2 comprises:

3 if the instruction does not indicate a known constant as a potential output value,
4 generating a micro-operation that receives a first potential output value as an input and also
5 receives a second potential output value as an input, wherein execution of the micro-
6 operation is to cause a processor to move either the first potential output value or the second
7 potential output value into a destination register.

1 29. The method of claim 25, wherein generating a plurality of predication-support
2 micro-operations further comprises:

3 generating an append micro-operation for each destination register indicated by the
4 instruction, wherein execution of the micro-operation is to cause a processor to append a
5 qualifying predicate for the instruction with a potential output value, and is to further cause
6 the appended value to be stored in a register.

1
1 30. An apparatus comprising:

2 a micro-operation generator to receive a predicated instruction, the predicated instruction
3 being one of a plurality of instructions, the plurality including arithmetic instructions and
4 memory instructions;

5 the micro-operation generator further to generate a plurality of micro-operations that
6 implement the instruction.

1
1 31. The apparatus of claim 30, wherein the predicated instruction is an arithmetic
2 instruction.

1
1 32. The apparatus of claim 31, wherein the predicated instruction is an add
2 instruction.

1 33. The apparatus of claim 31, wherein the predicated instruction is a compare
2 instruction.

1 34. The apparatus of claim 30, wherein the predicated instruction is a memory
2 instruction.

1 35. The apparatus of claim 34, wherein the predicated instruction is a load
2 instruction.

1 36. The apparatus of claim 34, wherein the predicated instruction is a store
2 instruction.

1 37. The apparatus of claim 30, wherein
2
3 the plurality of micro-operations includes one or more standard micro-operations to
4 provide the basic functionality indicated by the instruction.

1 38. The apparatus of claim 30, wherein
2 the plurality of micro-operations includes one or more predication-support micro-
3 operations.

1 39. The apparatus of claim 38, wherein:

1 the one or more predication-support micro-operations includes a conditional move micro-
2 operation for each destination register indicated by the instruction, where the conditional
3 move micro-operation is to select between a first and second proposed output value based on
4 the value of a qualifying predicate associated with the instruction.

5
1 40. The apparatus of claim 39, wherein:

2 the first proposed output value is the incoming value of the associated destination
3 register; and

4 the second proposed output value is a computed value.

5
1 41. The apparatus of claim 39, wherein:

2 the first proposed output value is the incoming value of the associated destination
3 register; and

4 the second proposed output value is a constant value.

1
1 42. The apparatus of claim 33, wherein the instruction is an “or” form compare
2 instruction.

3
3 43. The apparatus of claim 33, wherein the instruction is an “and” form compare
4 instruction.

5

1 44. The apparatus of claim 33, wherein the instruction is an “and”-complement form
2 compare instruction.

1 45. The apparatus of claim 33, wherein the instruction is an “or”-complement form
2 compare instruction.

1 46. The apparatus of claim 31, wherein:
2 the instruction is a parallel compare instruction.

1 47. The apparatus of claim 38, wherein:
2 the one or more predication-support micro-operations include a first conditional move
3 micro-operation for a first destination register indicated by a parallel compare instruction;
4 the one or more predication-support micro-operations also include a second conditional
5 move micro-operation for a second destination register indicated by the parallel compare
6 instruction;
7 the first proposed output value for the first conditional move micro-operation is the
8 incoming value of the associated destination register;
9 the second proposed output value for the first conditional move micro-operation is a first
10 constant;
11 the first proposed output value for the second conditional move micro-operation is the
12 incoming value of the associated destination register; and

the second proposed output value for second first conditional move micro-operation is a second constant.

48. The apparatus of claim 46, wherein the instruction is an “and.orcm” form of a parallel compare instruction.

49. The apparatus of claim 46, wherein the instruction is an “or.andcm” form of a parallel compare instruction.

50. The apparatus of claim 38, wherein:

the one or more predication support micro-operations includes an append operation to append a qualifying predicate value to a proposed output value.

51. The apparatus of claim 38, wherein:

the instruction is a load instruction; and

the one or more predication support micro-operations includes an append operation to append a qualifying predicate value to a load address.

52. The apparatus of claim 38, wherein:

2 the instruction is a store instruction; and
3 the one or more predication support micro-operations includes an append operation to
4 append a qualifying predicate value to a store address.

1
1 53. The apparatus of claim 30, wherein:
2 the micro-operation generator is further to decompose the instruction into the plurality of
3 micro-operations such that each of the micro-operations indicates a single destination
4 register.